Claims

What is claimed is:

1. An electronic system, comprising:

at least one processor;

a signal processing system coupled to the processor and operating in accordance with operational modes of the system, wherein the signal processing system includes,

an input sample subsystem coupled to the processor that receives data via at least one channel and produces input data samples;

a signal processing subsystem coupled to the processor, wherein the signal processing subsystem includes at least one matched filter having at least one configurable parameter automatically configured in accordance with the operational modes;

a fast Fourier transform (FFT) subsystem coupled to the processor and having at least one of a number of inputs and a transform size automatically configured in accordance with the operational modes; and

a memory subsystem automatically configurable into a plurality of configurations according to the operational modes.

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2. The system of claim 1, wherein the input sample subsystem automatically scales gain in response to a level of the received data.

3. The system of claim 1, wherein the input sample subsystem automatically controls decimation of the received data in accordance with the operational modes.

4. The system of claim 3, wherein the control of decimation includes at least one first decimation mode selected according to an amount of memory

consumed and at least one second decimation mode is selected according to an amount of the received data.

5. The system of claim 1, wherein the at least one configurable parameter of the matched filter includes a number of taps, a number of accumulations, and a tap offset.

6. The system of claim 1, wherein the signal processing subsystem generates coherent data.

7. The system of claim 1, further comprising a coherent accumulator coupled to receive outputs of the matched filter.

8. The system of claim 1, wherein the memory subsystem is configurable into regions, wherein each region stores a type of data, and each region is accessed in one of a plurality of manners, and each region is accessed by particular subsystems, and wherein at least one of the regions stores data words from the processor that determine the configuration of the memory subsystem, including sizes of different regions, and manners of access to be used for accessing particular regions.

9. The system of claim 1, further comprising at least one sequencer coupled to the processor that automatically controls time multiplexed use of at least one of the input sample subsystem, signal processing subsystem, and the FFT subsystem among the channels.

10. The system of claim 9, wherein the sequencer controls processing of data from the channels by controlling channel access to at least one of the input sample subsystem, signal processing subsystem, and the FFT subsystem in accordance with at least one rule.

11. The system of claim 9, wherein the sequencer automatically configures at least one of the signal processing subsystem and the FFT subsystem using information from the memory subsystem.

12. The system of claim 1, further comprising at least one first controller that controls storage of data from the signal processing subsystem using an optimal pattern, wherein the optimal pattern stores data from the signal processing subsystem so as to allow simultaneous access to the data by the FFT subsystem while avoiding collisions among the accessed data.

13. The system of claim 1, further comprising at least one second controller coupled among the input sample subsystem and the signal processing subsystem to control access to the memory subsystem.

14. The system of claim 1, further comprising at least one third controller coupled among the signal processing subsystem, the FFT subsystem, and the memory subsystem.

15. The system of claim 14, wherein the third controller controls transfer of data among the signal processing subsystem and the FFT subsystem.

16. The system of claim 1, further comprising at least one non-coherent accumulator coupled to receive data from the FFT subsystem.

17. The system of claim 1, wherein the memory subsystem comprises a first memory area coupled for access by a first processor via a first bus, a second memory area coupled for access by a second processor via a second bus, wherein the plurality of configurations include configurations that provide shared access of the second memory area by the first processor, and access by the first processor to a first

set of memory locations of the second memory area via the first bus and access by the first processor to a second set of memory locations of the second memory area via the second bus.

18. The system of claim 1, further comprising a first receiver that includes a first clock generating a first clock signal, a second receiver that includes a second clock generating a second clock signal, at least one area of the memory subsystem that stores values representative of the first and second clock signals, and a ratio counter that generates a control signal in accordance with one of the values, counts pulses of the first clock signal and the second clock signal and captures the count of each clock signal in response to the control signal, and determines a ratio between frequencies of the first and second clock signals using the count.

19. The system of claim 1, wherein the signal processing system is configurable to process satellite signal data in a satellite-based positioning system.

20. The system of claim 1, wherein the signal processing is configurable to process at least one other signal from a terrestrial transmitter.

21. The system of claim 1, wherein the data comprises global positioning system (GPS) satellite signals, and wherein the operational modes include at least one of modes in which a wide, low-resolution search for GPS satellites is performed, modes in which a narrow, high resolution search for GPS satellites is performed, and modes in which previously acquired GPS satellites are tracked.

22. The system of claim 1, wherein the operational modes include a cold start mode, a coarse acquisition mode, a hot start mode, and a track mode.

23. The system of claim 1, wherein the memory subsystem is configurable into regions that include an input sample memory that stores input data samples, a coherent memory that stores coherent data, and a noncoherent summation (NCS) memory that stores noncoherent data.

24. The system of claim 1, wherein the plurality of configurations include a cold start configuration that corresponds to a first operational mode, wherein the memory subsystem is configurable into regions that include an input sample memory, and an NCS memory, wherein the input sample memory is of significantly greater size than the NCS memory, wherein the input sample memory is filled with input data samples in a one-shot manner such that the signal processing subsystem processes data in the filled input sample memory at least once before the data is overwritten.

25. The system of claim 24, wherein in the first operational mode, the signal processing system produces coherent data and transmits the coherent data to the FFT subsystem, wherein the FFT subsystem produces noncoherent data and stores the noncoherent data in the NCS memory.

26. The system of claim 1, wherein the plurality of configurations include a coarse acquisition configuration that corresponds to a second operational mode, wherein the memory subsystem is configurable into regions that include an input sample memory, a coherent memory, and an NCS memory, wherein the NCS memory is of significantly greater size than either of the input sample memory and the coherent memory, wherein the input sample memory is filled with input data samples in a cyclic manner such that the signal processing subsystem reads out data to be processed from one area of the input sample memory while the input sample subsystem writes data into the input sample memory.

27. The system of claim 26, wherein in the second operational mode, the signal processing subsystem produces coherent data and stores the coherent data in the coherent memory while the FFT subsystem reads coherent data out of the coherent memory.

28. The system of claim 1, wherein the plurality of configurations include a hot start configuration that corresponds to a third operational mode, wherein the memory subsystem is configurable into regions that include an input sample memory, a coherent memory, and an NCS memory, wherein the NCS memory is of significantly greater size than either of the input sample memory and the coherent memory, wherein the input sample memory is filled with input data samples in a cyclic manner such that the signal processing subsystem reads out data to be processed from one area of the input sample memory while the input sample subsystem writes data into the input sample memory, wherein the signal processing subsystem produces coherent data and stores the coherent data in the coherent memory, wherein the coherent memory is configured to include a scratch area and a plurality of coherent areas, each for storage of coherent data from a satellite.

29. The system of claim 28, wherein in the third operational mode, the signal processing subsystem writes coherent data into the coherent memory while the FFT subsystem reads coherent data out of the coherent memory.

30. The system of claim 1, wherein the plurality of configurations include a tracking configuration that corresponds to a fourth operational mode, wherein the memory subsystem is configurable into regions that include an input sample memory, a coherent memory, and an NCS memory, wherein the NCS memory is of significantly greater size than either of the input sample memory and the coherent memory, wherein the input sample memory is filled with input data samples in a cyclic manner such that the signal processing subsystem reads out data to be

processed from one area of the input sample memory while the input sample subsystem writes data into the input sample memory, wherein the signal processing subsystem produces coherent data and stores the coherent data in the coherent memory, wherein the FFT subsystem reads coherent data out of the coherent memory, and produces noncoherent data and stores the noncoherent data in the NCS memory, wherein the NCS memory is configured to include an NCS region and a peak region, and a track region.

31. The system of claim 1, wherein the electronic system includes at least one of cellular telephones, portable telephones, portable communication devices, personal computers, portable computing devices, and personal digital assistants.

32. An electronic system, comprising at least one processor and a signal processing system coupled to operate under a plurality of operational modes, wherein the signal processing system includes a signal processing subsystem and a fast Fourier transform (FFT) subsystem that are automatically and dynamically configurable in response to the operational modes, wherein the signal processing subsystem includes at least one matched filter having at least one configurable parameter automatically configured in accordance with the operational modes, wherein the fast Fourier transform (FFT) subsystem includes at least one of a number of inputs and a transform size automatically configured in accordance with the operational modes.

33. The system of claim 32, further comprising an input sample subsystem coupled to the processor that receives data via at least one channel and produces input data samples.

34. The system of claim 32, further comprising a memory subsystem that is automatically and dynamically configurable into a plurality of configurations according to the operational modes, wherein the memory subsystem is configurable

into regions, wherein each region stores a type of data, and each region is accessed in one of a plurality of manners, and each region is accessed by particular subsystems, and wherein at least one of the regions stores data words from the processor that determine the configuration of the memory subsystem, including sizes of different regions, and manners of access to be used for accessing particular regions.

35. The system of claim 32, wherein the at least one configurable parameter of the matched filter includes a number of taps, a number of accumulations, and a tap offset.

36. The system of claim 32, further comprising at least one sequencer coupled to the processor that automatically and dynamically controls time multiplexed use of at least one of the signal processing subsystem and the FFT subsystem among the channels by controlling channel access to at least one of the signal processing subsystem and the FFT subsystem in accordance with at least one rule, wherein the sequencer automatically configures at least one of the signal processing subsystem and the FFT subsystem using information from at least one memory area.

37. The system of claim 32, further comprising at least one first controller that controls storage of data from the signal processing subsystem using an optimal pattern, wherein the optimal pattern stores data from the signal processing subsystem so as to allow simultaneous access to the data by the FFT subsystem while avoiding collisions among the accessed data.

38. The system of claim 32, further comprising at least one second controller coupled among the signal processing subsystem, the FFT subsystem, and a configurable memory subsystem to control transfer of data among the signal processing subsystem and the FFT subsystem.

39. The system of claim 32, wherein the signal processing system is configurable to process satellite signal data in a satellite-based positioning system.

40. The system of claim 39, wherein the data comprises global positioning system (GPS) satellite signals, and wherein the operational modes include at least one of modes in which a wide, low-resolution search for GPS satellites is performed, modes in which a narrow, high resolution search for GPS satellites is performed, and modes in which previously acquired GPS satellites are tracked.

41. The system of claim 32, wherein the operational modes include a cold start mode, a coarse acquisition mode, a hot start mode, and a track mode.

42. The system of claim 32, wherein the electronic system includes at least one of cellular telephones, portable telephones, portable communication devices, personal computers, portable computing devices, and personal digital assistants.

43. An electronic system, comprising at least one processor and a signal processor operating according to a plurality of operational modes, wherein the signal processor includes a signal processing subsystem, a fast Fourier transform (FFT) subsystem, and a memory subsystem that are each dynamically and independently configurable in response to the operational modes, wherein a first controller couples to control transfer of data among the signal processing subsystem and the FFT subsystem via the memory subsystem, wherein configurability of the memory subsystem includes configuring the memory subsystem into regions according to the operational modes, wherein the regions are each accessible in one of a plurality of manners according to the operational modes.

44. The system of claim 43, wherein the signal processing subsystem includes at least one matched filter having at least one configurable parameter

automatically configured in accordance with the operational modes, wherein the fast Fourier transform (FFT) subsystem includes at least one of a number of inputs and a transform size automatically configured in accordance with the operational modes.

45. The system of claim 43, further comprising an input sample subsystem coupled to receive data via at least one channel and generate input data samples, wherein the data comprises global positioning system (GPS) satellite signals, and wherein the operational modes include at least one of modes in which a wide, low-resolution search for GPS satellites is performed, modes in which a narrow, high resolution search for GPS satellites is performed, and modes in which previously acquired GPS satellites are tracked.

46. The system of claim 43, wherein at least one of the regions stores data words from the processor that determine the configuration of the memory subsystem, including sizes of different regions, and manners of access to be used for accessing particular regions.

47. The system of claim 43, further comprising at least one second controller that controls storage of data from the signal processing subsystem using an optimal pattern that stores data from the signal processing subsystem so as to allow simultaneous access to data of a plurality of locations in the memory subsystem by the FFT subsystem while avoiding collisions among the accessed data.

48. The system of claim 43, wherein the electronic system includes at least one of cellular telephones, portable communication devices, and portable computing devices.

49. The system of claim 1, further includes:

a serial interface between the signal processing system and the input sample subsystem.

50. The system of claim 1, further includes:

a twiddle algorithm in receipt of output data from the signal processing system that stores in the memory the output in a pattern that is accessed by the fast Fourier subsystem.

51. An electronic system, comprising:

means for controlling processing;

means for processing signals coupled to the means for controlling processing and operating in accordance with operational modes of the system, the means for processing signals including,

means for receiving data and producing input data samples;

means for generating coherent data using the input data samples, wherein the means for generating coherent data includes at least one matched filter means having at least one configurable parameter automatically configured in accordance with the operational modes;

means for generating fast Fourier transforms (FFTs) having at least one of a number of inputs and a transform size automatically configured in accordance with the operational modes; and

means for storing data that is automatically configurable into a plurality of configurations according to the operational modes.

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